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B. Amendments to the Specification.

Please replace the paragraph starting at Page 5, Line 4, with the following.

a1 5 While a conventional assembly ~~600~~ 800 such as that shown in FIGS. 8A to 8C can provide BIST functionality, it comes at the cost of increased circuit area on a PLD 804.

Please replace the paragraph starting at Page 5, Line 9, with the following.

a2 10 It would be desirable to arrive at some way of implementing self-test on a programmable logic device that can be more economical than conventional approaches.

Please replace the paragraph starting at Page 8, Line 8, with the following.

a3 15 As shown in FIG. 3, a method 300 may include providing an assembly that includes a nonvolatile memory and volatile PLD (step 302). FIG. 2A shows an assembly 200 that includes a nonvolatile memory 202, a volatile PLD 204, and a test port 206. In one particular arrangement, a nonvolatile memory 202 may include an electrically erasable and programmable read-only-memory (EEPROM), such as a "flash" EEPROM. In addition, a volatile PLD 204
20 may be formed on a different integrated circuit die than a nonvolatile memory 202. As but a two of the many possible arrangements, a volatile PLD 204 and nonvolatile memory 202 may be different dice assembled in the same package (e.g., multi-chip module, or the like). Alternatively, a volatile PLD 204 and nonvolatile memory 202 may be in different packages on the same circuit board.

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Please replace the paragraph starting at Page 13, Line 1, with the following.

a4 30 By storing BIST data in a second nonvolatile memory ~~402~~ 410, an assembly 400 according to a second embodiment can provide BIST capabilities with relatively small increases in die size with respect to conventional approaches that include hard logic for BIST capabilities.

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a4 In this way, built-in-self-test capabilities can be provided without substantially increasing the size of a programmable logic device.

Please replace the paragraph starting at Page 11, Line 6, with the following.

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a5 While BIST data may be programmed into a nonvolatile memory device, such data may be established at an earlier point in the manufacturing process, resulting in BIST data that may be stored in a more permanent fashion. Such an arrangement is illustrated in a second embodiment shown in FIGS. 4A, 4B and 5. FIG. 5 is a flow diagram describing a method of testing a PLD according to a second embodiment. FIGS. 4A and 4B are diagrams corresponding to the method illustrated in FIG. 3 5.

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